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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,819	10/07/2004	Matthew Breitwisch	BUr920040054US1	5818

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EXAMINER	
LE, TOAN K	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 03/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,819	BREITWISCH ET AL.	
	Examiner	Art Unit	
	Toan Le	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-10,14-17,19 and 20 is/are rejected.

7)☒ Claim(s) 11-13 and 18 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 07 October 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 6/24/05; 10/7/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: East search history.

DETAILED ACTION

Information Disclosure Statement

1. This office acknowledge receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on June 24, 2005.

Information Disclosure Statement (IDS) filed on October 07, 2004.

2. Information disclosed and list on PTO 1449 was considered.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-10, 14-17 and 19-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Chindalore et al. (U.S. 6,839,280).

Regarding claims 8- 10, 14-17 and 19-20, Chindalore et al. disclose a CMOS integrated circuit comprising a plurality of nonvolatile storage cells (memory cell array 32 of figs. 3 and 5) embedded in logic on the integrate circuit (see figs 5-11); ones of the storage cells (50 of fig. 4) being selectively coupled to a first input of a differential sense amplifier (40 of figs. 3 and 4); and a variable reference signal (I_{REF}) coupled to a second input of the amplifier (see fig. 4), the

variable reference signal having a plurality of selectable reference levels corresponding to reprogrammed cell threshold voltages (see col. 4, lines 17-23), wherein with each write cycle a different one of the selectable reference levels is coupled to the second input (see col. 3, lines 45-50 and col. 4, lines 16-24), and contents of the storage cells subsequently being compared with the different one by the amplifier (see col. 1, lines 28-30 and col.4, lines 44-50). Chindalore et al. further disclose a dummy cell (46 of fig. 4 and see col. 1, lines 40-50) having a threshold voltage programmed with each write cycle at least at a current cell threshold voltage (see col. 4, lines 16-33) below a reprogrammed cell threshold voltage (see fig. 2), wherein at least one of the storage cells have a programmed cell threshold voltage and remaining ones of the storage cells have an unprogrammed cell threshold voltage (erased cell threshold voltage) which is below the programmed cell threshold voltage (see fig. 2 and see col. 4, lines 50-55). Also, Fig. 3 shows a word decoder (36) partially selecting ones of the storage cells connected to one of a plurality of word lines (see col. 3, lines 32-35) and a bit decoder (column decoder 34) selectively coupling partially selected the ones to the first input of the amplifier (col. 3, lines 32-35, lines 47-50; and see fig. 3).

Regarding claims 1-7, the apparatus as described above would perform a method of programming nonvolatile memory cells as recited in claims 1-7.

Allowable Subject Matter

5. Claims 11-13 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: The prior art does not teach or suggest an integrated circuit comprising an active dummy load device for loading the dummy cell, in combination with the remaining claimed limitation as recited in claim 11 and 18.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Eshel (US. 6,937,523) discloses a method and apparatus for sensing the programmed/erased state of a selected memory cell.

Tanzawa (US 6,818,413) discloses a multilevel flash memory.

Pasotti et al. (U.S. 6,535,428) disclose a sensing circuit for memory cells.

Camerlenghi et al. (U.S. 5,576,990) disclose a voltage regulator for nonvolatile memory devices.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toan Le whose telephone number is (571) 272-1872. The examiner can normally be reached on M-F (8.00AM - 5.30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

3/4/06

TL
February 28, 2006